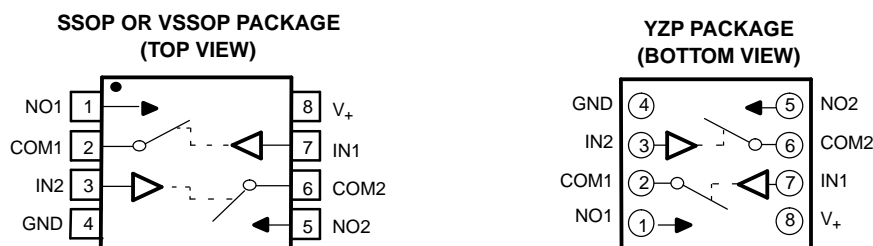


## FEATURES

- Isolation in Powered-Down Mode,  $V_+ = 0$
- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

## APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



## DESCRIPTION/ORDERING INFORMATION

The TS5A23166 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		TS5A23166YZPR	JM7
	SSOP – DCT	Tape and reel	TS5A23166DCTR	PACKAGE PREVIEW
	VSSOP – DCU (Pb-free)	Tape and reel	TS5A23166DCUR	JAM_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).
- (2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
DCU: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TS5A23166**  
**0.9-Ω DUAL SPST ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL ANALOG SWITCH**

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**SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	Dual Single Pole, Single Throw (2 × SPST)
Number of channels	2
ON-state resistance ( $r_{on}$ )	0.9 Ω
ON-state resistance match ( $\Delta r_{on}$ )	0.1 Ω
ON-state resistance flatness ( $r_{on(Flat)}$ )	0.25 Ω
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	7.5 ns/9 ns
Charge injection ( $Q_C$ )	6 pC
Bandwidth (BW)	150 MHz
OFF isolation ( $O_{ISO}$ )	–62 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	–85 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ( $I_{COM(OFF)}$ )	±20 nA
Power-supply current ( $I_+$ )	0.1 μA
Package options	8-pin SSOP, VSSOP, and WCSP

(1)  $V_+ = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**FUNCTION TABLE**

IN	NO TO COM, COM TO NO
L	OFF
H	ON

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	–0.5	6.5	V
$V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3)(4)(5)</sup>	–0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current	$V_{NO}, V_{COM} < 0$		mA
$I_{NO}$ $I_{COM}$	On-state switch current On-state peak switch current <sup>(6)</sup>	$V_{NO}, V_{COM} = 0$ to $V_+$		mA
$V_I$	Digital input voltage range <sup>(3)(4)</sup>	–0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	–100	100	mA
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>	DCT package		220
		DCU package		227
		YZP package		102
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup>**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.9	1.1	$\Omega$	
				Full		1.2			
ON-state resistance	$r_{on}$	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.75	0.9	$\Omega$	
				Full		1			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.04	0.1	$\Omega$	
				Full		0.1			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See Figure 13	25°C	4.5 V	0.2		$\Omega$	
				25°C		0.15	0.25		
				Full		0.25			
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		-150	150		
	$I_{NO(PWROFF)}$	$V_{NO} = 0\text{ to }5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to }0$ ,	Switch OFF, See Figure 14	25°C	0 V	-10	0.2	10	$\mu\text{A}$
				Full		-50	50		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NO} = 1\text{ V}$ ,	Switch OFF, See Figure 14	25°C	5.5 V	0 V	4	20	nA
				Full		-150	150		
	$I_{COM(PWROFF)}$	$V_{COM} = 0\text{ to }5.5\text{ V}$ , $V_{NO} = 5.5\text{ V to }0$ ,	Switch OFF, See Figure 14	25°C	0 V	-10	0.2	10	$\mu\text{A}$
				Full		-50	50		
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-5	0.4	5	nA
				Full		-50	50		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	5.5 V	-5	0.4	5	nA
				Full		-50	50		
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full		2.4		5.5	V	
Input logic low	$V_{IL}$		Full		0		0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	5.5 V	-2	0.3	2	nA	
			Full		-20	20			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

 (2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	1	4.5	7.5	ns
			Full	4.5 V to 5.5 V	1		9	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	5 V	4.5	8	11	ns
			Full	4.5 V to 5.5 V	3.5		13	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See Figure 21	25°C	5 V		6		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	5 V		18		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	5 V		35.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	5 V		35.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	5 V		150		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See Figure 19	25°C	5 V		-62		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See Figure 20	25°C	5 V		-85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	5 V		0.005		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V		0.01	0.1	$\mu\text{A}$
			Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See Figure 13	25°C	3 V	1.3		1.6	$\Omega$
			Full				1.8	
ON-state resistance	$r_{on}$	$V_{NO} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See Figure 13	25°C	3 V	1.1		1.5	$\Omega$
			Full				1.7	
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See Figure 13	25°C	3 V	0.04		0.1	$\Omega$
			Full				0.1	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See Figure 13	25°C	3 V	0.3			$\Omega$
			25°C		0.15		0.25	
			Full				0.25	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1\text{ V}, V_{COM} = 3\text{ V}$ , or $V_{NO} = 3\text{ V}, V_{COM} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C	3.6 V	-5	0.5	5	nA
			Full				50	
	$I_{NO(PWROFF)}$	$V_{NO} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ , Switch OFF, See Figure 14	25°C	0 V	-5	0.1	5	$\mu\text{A}$
			Full				25	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}, V_{NO} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}, V_{NO} = 1\text{ V}$ , Switch OFF, See Figure 14	25°C	3.6 V	-5	0.5	5	nA
			Full				50	
	$I_{COM(PWROFF)}$	$V_{COM} = 0\text{ to }3.6\text{ V}$ , $V_{NO} = 3.6\text{ V to }0$ , Switch OFF, See Figure 14	25°C	0 V	-5	0.1	5	$\mu\text{A}$
			Full				25	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 3\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C	3.6 V	-2	0.3	2	nA
			Full				20	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} = \text{Open}$ , Switch ON, See Figure 15	25°C	3.6 V	-2	0.3	2	nA
			Full				20	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		2		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	3.6 V	-2	0.3	2	nA
			Full				20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)**

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	1.5	5	9.5	ns
			Full	3 V to 3.6 V	1		10	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	3.3 V	4.5	8.5	11	ns
			Full	3 V to 3.6 V	3		12.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See Figure 21	25°C	5 V		6		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	3.3 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	3.3 V		18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	3.3 V		36		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	3.3 V		150		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See Figure 19	25°C	3.3 V		-62		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See Figure 20	25°C	3.3 V		-85		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	3.3 V		0.01		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V	0.001	0.05		$\mu\text{A}$
			Full			0.3		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.8	2.4	$\Omega$
				Full				
ON-state resistance	$r_{on}$	$V_{NO} = 1.8 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	1.2	2.1	$\Omega$
				Full				
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.8 \text{ V}$ , 0.8 V, $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	0.04	0.15	$\Omega$
				Full				
ON-state resistance flatness	$r_{on (flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$ ,	Switch ON, See Figure 13	25°C	2.3 V	0.7	0.6	$\Omega$
				25°C				
				Full				
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0.5 \text{ V}$ , $V_{COM} = 2.3 \text{ V}$ , or $V_{NO} = 2.3 \text{ V}$ , $V_{COM} = 0.5 \text{ V}$ ,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5
				Full				
	$I_{NO(PWROFF)}$	$V_{NO} = 0 \text{ to } 2.7 \text{ V}$ , $V_{COM} = 2.7 \text{ V to } 0$ ,	Switch OFF, See Figure 14	25°C	0 V	-2	0.05	2
				Full				
COM OFF leakage current	$I_{COM(OFF)}$	$V_{NO} = 2.3 \text{ V}$ , $V_{COM} = 0.5 \text{ V}$ , or $V_{NO} = 0.5 \text{ V}$ , $V_{COM} = 2.3 \text{ V}$ ,	Switch OFF, See Figure 14	25°C	2.7 V	-5	0.3	5
				Full				
	$I_{COM(PWROFF)}$	$V_{COM} = 0 \text{ to } 2.7 \text{ V}$ , $V_{NO} = 2.7 \text{ V to } 0$ ,	Switch OFF, See Figure 14	25°C	0 V	-2	0.05	2
				Full				
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.5 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 2.3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2
				Full				
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 0.5 \text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 2.3 \text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, See Figure 15	25°C	2.7 V	-2	0.3	2
				Full				
<b>Digital Control Inputs (IN1, IN2)</b>								
Input logic high	$V_{IH}$		Full		1.8		5.5	V
Input logic low	$V_{IL}$		Full		0		0.6	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C	2.7 V	-2	0.3	2	$\text{nA}$
			Full					

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

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**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)**

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	2	6	10	ns
			Full	2.3 V to 2.7 V	1		12	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ , See Figure 17	25°C	2.5 V	4.5	8	12.5	ns
			Full	2.3 V to 2.7 V	3		15	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1 \text{ nF}$ , See Figure 21	25°C	2.5 V		4		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	2.5 V		18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON, See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ , Switch OFF, See Figure 19	25°C	2.5 V		-62		dB
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ , Switch ON, See Figure 20	25°C	2.5 V		-85		dB
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , See Figure 22	25°C	2.5 V		0.02		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	2.7 V		0.001	0.02	$\mu\text{A}$
			Full				0.25	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.



**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See Figure 13	25°C	1.65 V	4.2		25	$\Omega$
			Full				30	
ON-state resistance	$r_{on}$	$V_{NO} = 0.6\text{ V}, 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See Figure 13	25°C	1.65 V	1.6		3.9	$\Omega$
			Full				4	
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See Figure 13	25°C	1.65 V	0.04		0.2	$\Omega$
			Full				0.2	
ON-state resistance flatness	$r_{on (flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See Figure 13	25°C	1.65 V	2.8			$\Omega$
			Full				27	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0.3\text{ V}$ , $V_{COM} = 1.65\text{ V}$ , or $V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V}$ , Switch OFF, See Figure 14	25°C	1.95 V	-5	0.3	5	nA
			Full				-50	
	$I_{NO(PWROFF)}$	$V_{NO} = 0\text{ to }1.95\text{ V}$ , $V_{COM} = 1.95\text{ V to }0$ , Switch OFF, See Figure 14	25°C	0 V	-2	0.05	2	$\mu\text{A}$
			Full				-10	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NO} = 0.3\text{ V}$ , $V_{COM} = 1.65\text{ V}$ , Switch OFF, See Figure 14	25°C	1.95 V	-5	0.3	5	nA
			Full				-50	
	$I_{COM(PWROFF)}$	$V_{COM} = 0\text{ to }1.95\text{ V}$ , $V_{NO} = 1.95\text{ V to }0$ , Switch OFF, See Figure 14	25°C	0 V	-2	0.05	2	$\mu\text{A}$
			Full				-10	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0.3\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 1.65\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See Figure 15	25°C	1.95 V	-2	0.3	2	nA
			Full				-20	
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NO} = \text{Open}$ , $V_{COM} = 1.65\text{ V}$ , Switch ON, See Figure 15	25°C	1.95 V	-2	0.3	2	nA
			Full				-20	
<b>Digital Control Inputs (IN1, IN2)</b>								
Input logic high	$V_{IH}$		Full		1.5		5.5	V
Input logic low	$V_{IL}$		Full		0		0.6	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	1.95 V	-2	0.3	2	$\mu\text{A}$
			Full				-20	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**TS5A23166**  
**0.9-Ω DUAL SPST ANALOG SWITCH**  
**5-V/3.3-V 2-CHANNEL ANALOG SWITCH**

SCDS196B–MAY 2005–REVISED FEBRUARY 2006

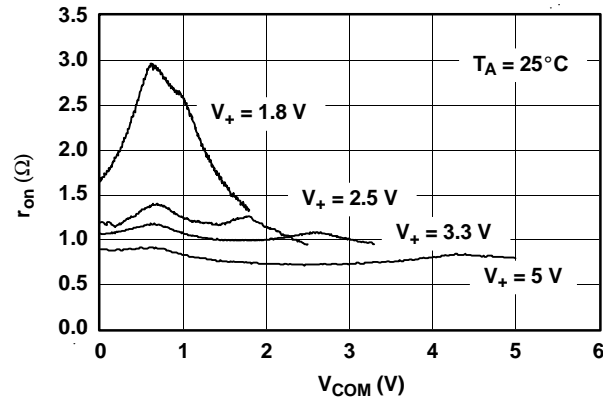
**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)**

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

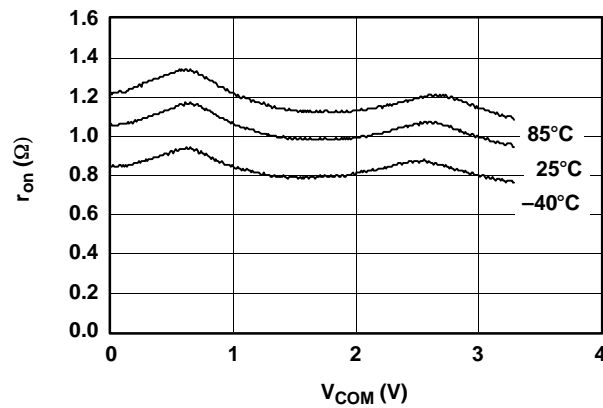
PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	3	9	18	ns
			Full	1.65 V to 1.95 V	1		20	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See Figure 17	25°C	1.8 V	5	10	15.5	ns
			Full	1.65 V to 1.95 V	4		18.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See Figure 21	25°C	1.8 V		2		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See Figure 16	25°C	1.8 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF, See Figure 16	25°C	1.8 V		18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See Figure 18	25°C	1.8 V		150		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See Figure 19	25°C	1.8 V		-62		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See Figure 22	25°C	1.8 V		0.055		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V		0.001	0.01	$\mu\text{A}$
			Full				0.15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

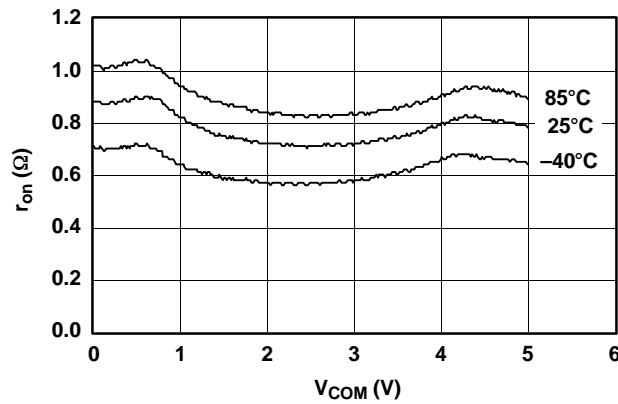
**TYPICAL PERFORMANCE**



**Figure 1.  $r_{on}$  vs  $V_{COM}$**



**Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3\text{ V}$ )**



**Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5\text{ V}$ )**

TYPICAL PERFORMANCE

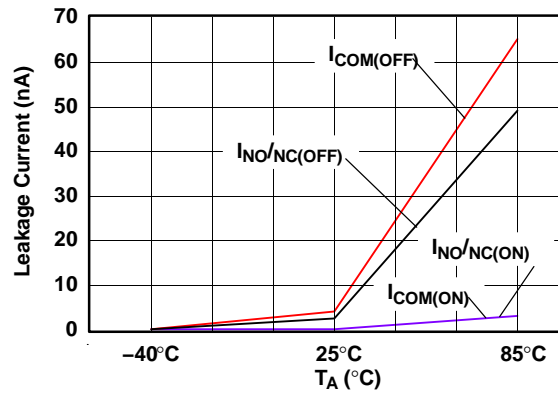


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5\text{ V}$ )

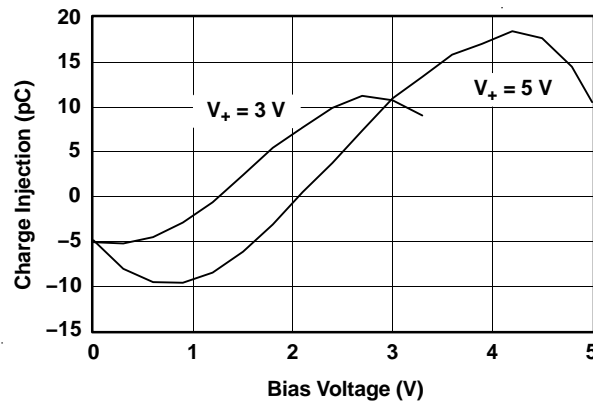


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

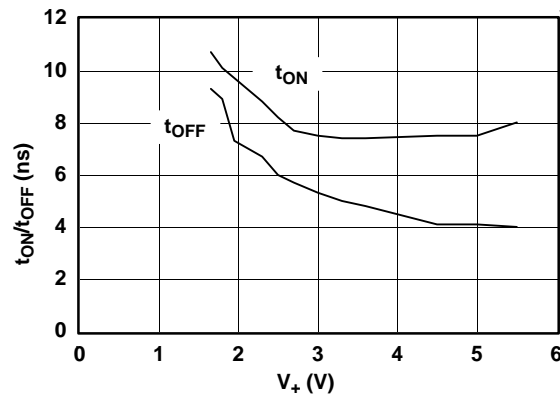
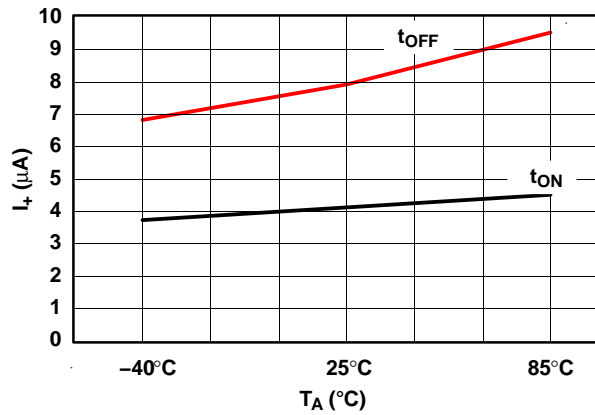
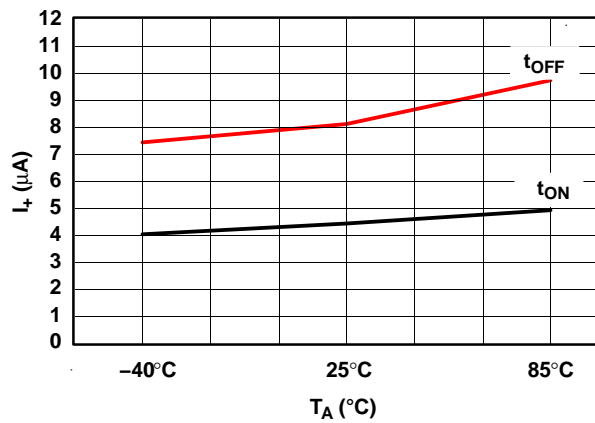


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

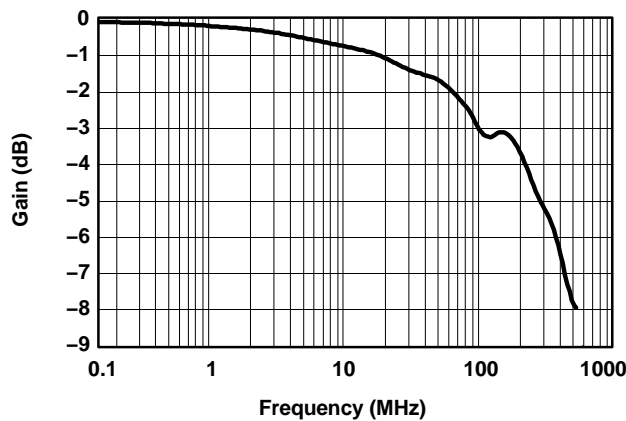
**TYPICAL PERFORMANCE**



**Figure 7. t<sub>ON</sub> and t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 5 V)**



**Figure 8. Logic-Level Threshold vs V<sub>+</sub>**



**Figure 9. Bandwidth (V<sub>+</sub> = 5 V)**

TYPICAL PERFORMANCE

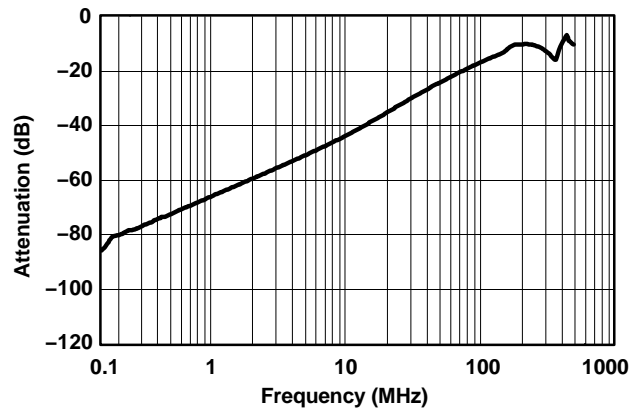


Figure 10. OFF Isolation and Crosstalk ( $V_+ = 5\text{ V}$ )

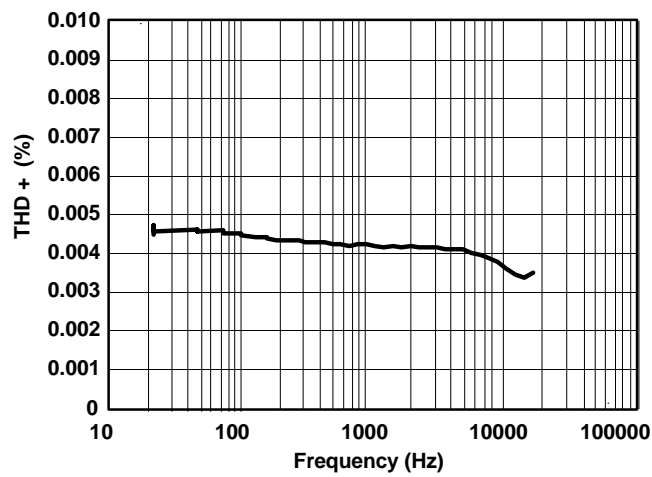


Figure 11. Total Harmonic Distortion vs Frequency

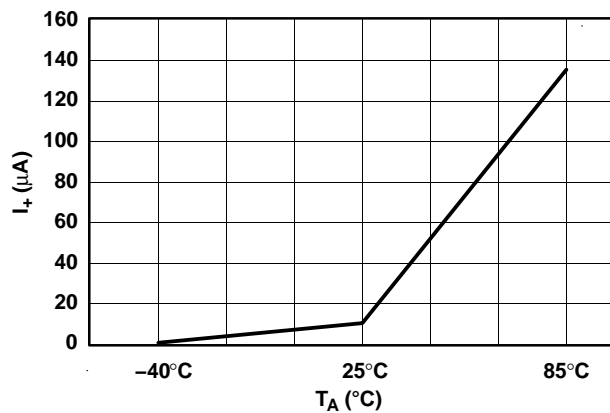


Figure 12. Power-Supply Current vs Temperature ( $V_+ = 5\text{ V}$ )

**PIN DESCRIPTION**

PIN NUMBER	NAME	DESCRIPTION
1	NO1	Normally closed
2	COM1	Common
3	IN2	Digital control pin to connect COM to NO
4	GND	Digital ground
5	NO2	Normally closed
6	COM2	Common
7	IN1	Digital control pin to connect COM to NO
8	V <sub>+</sub>	Power Supply

**PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
V <sub>COM</sub>	Voltage at COM
V <sub>NO</sub>	Voltage at NO
r <sub>on</sub>	Resistance between COM and NO ports when the channel is ON
r <sub>on(flat)</sub>	Difference between the maximum and minimum value of r <sub>on</sub> in a channel over the specified range of conditions
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
I <sub>COM(OFF)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V <sub>IH</sub>	Minimum input voltage for logic high for the control input (IN)
V <sub>IL</sub>	Maximum input voltage for logic low for the control input (IN)
V <sub>I</sub>	Voltage at the control input (IN)
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN)
t <sub>ON</sub>	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t <sub>OFF</sub>	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, Q <sub>C</sub> = C <sub>L</sub> × ΔV <sub>COM</sub> , C <sub>L</sub> is the load capacitance and ΔV <sub>COM</sub> is the change in analog output voltage.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
C <sub>COM(OFF)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C <sub>I</sub>	Capacitance of IN
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I <sub>+</sub>	Static power-supply current with the control (IN) pin at V <sub>+</sub> or GND
ΔI <sub>+</sub>	This is the increase in I <sub>+</sub> for each control (IN) input that is at the specified voltage, rather than at V <sub>+</sub> or GND.

PARAMETER MEASUREMENT INFORMATION

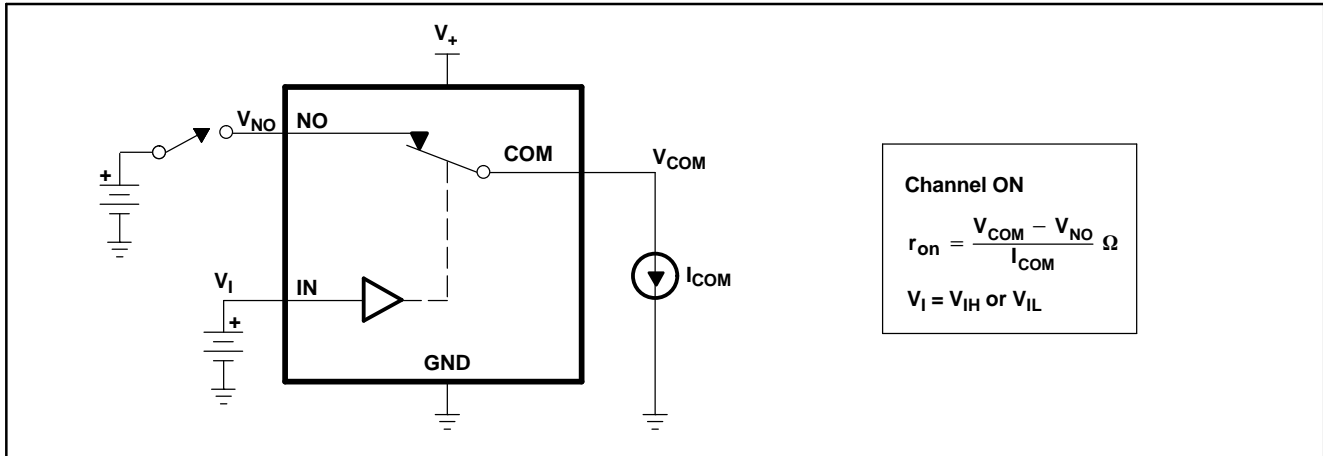


Figure 13. ON-State Resistance ( $r_{on}$ )

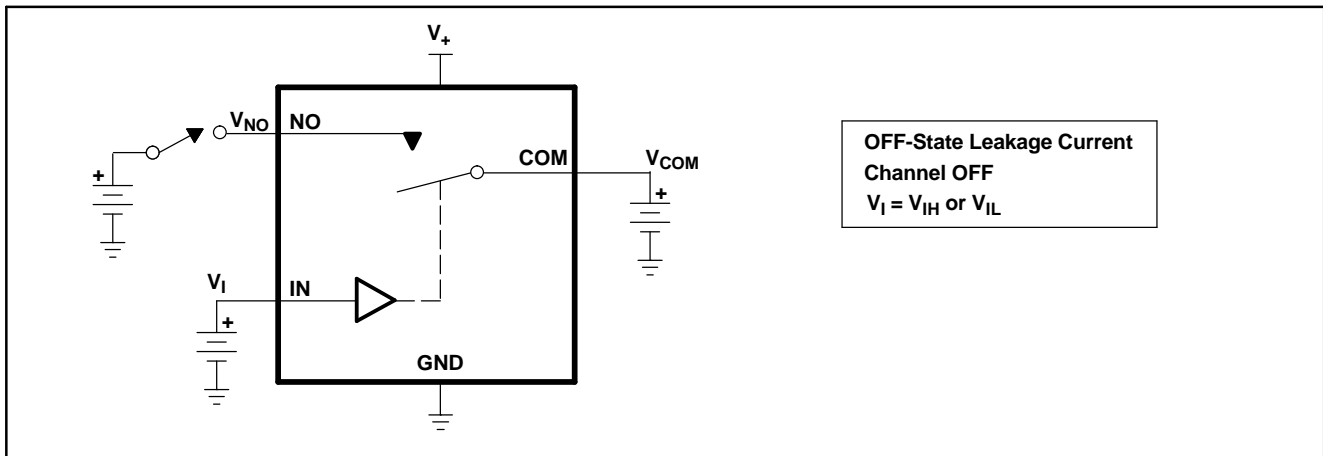


Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NC(PWR(F))}$ )

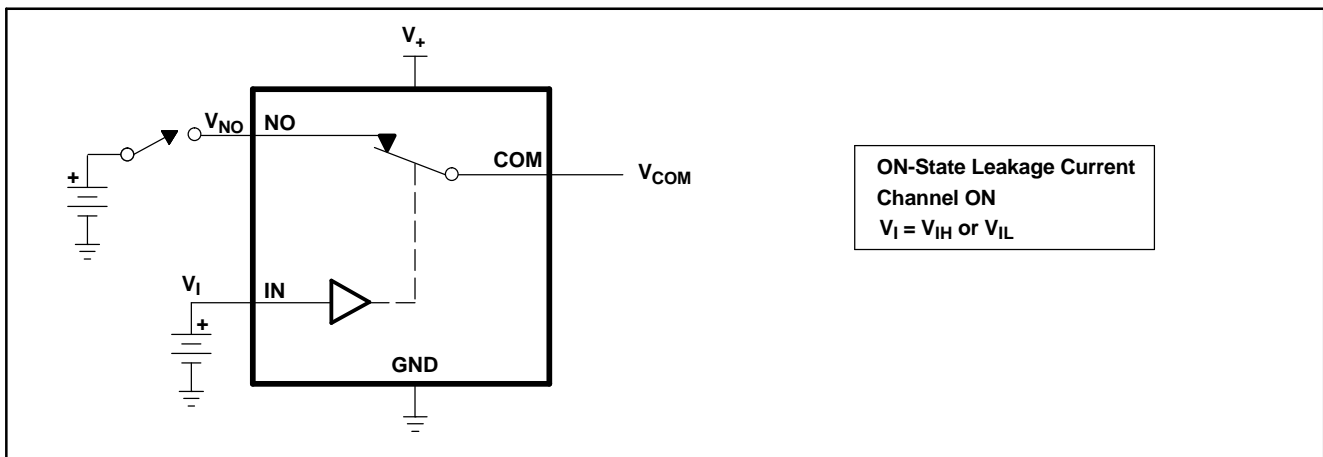


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )



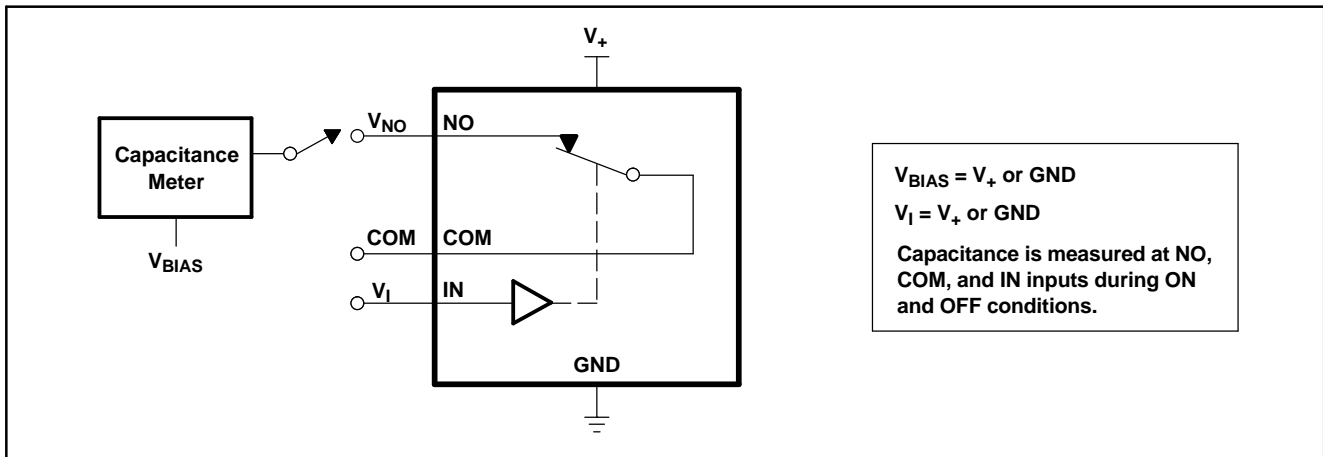
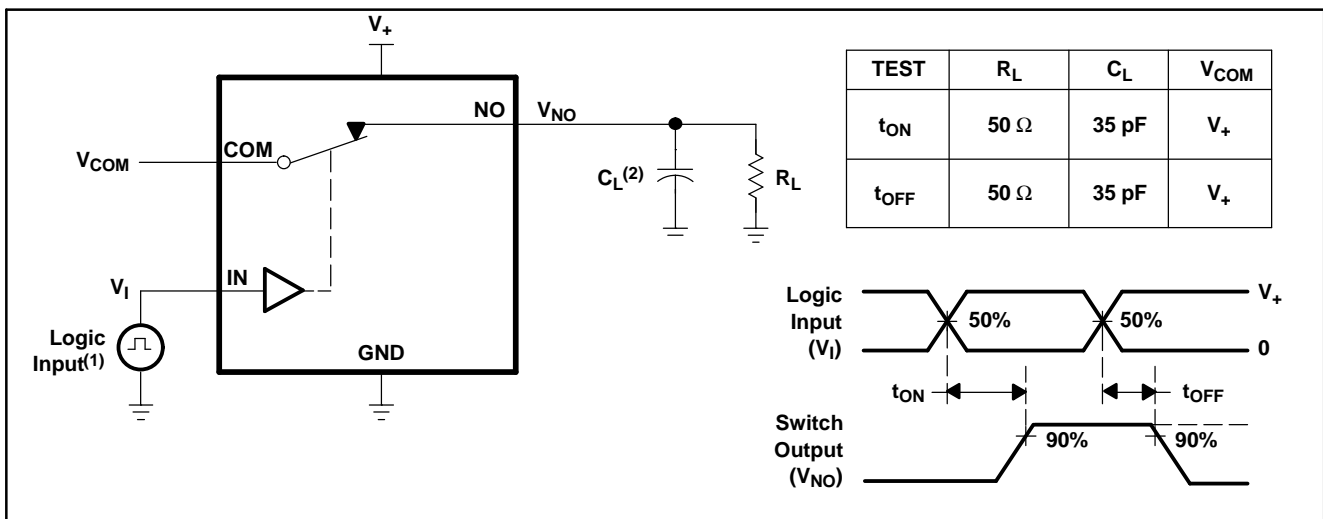


Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

(2)  $C_L$  includes probe and jig capacitance.

Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )

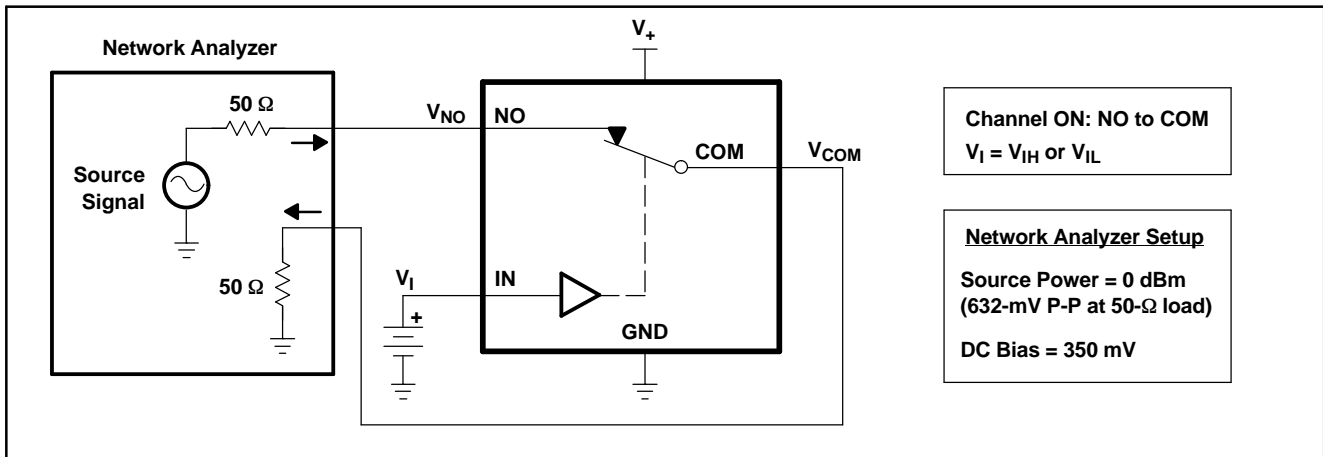


Figure 18. Bandwidth (BW)

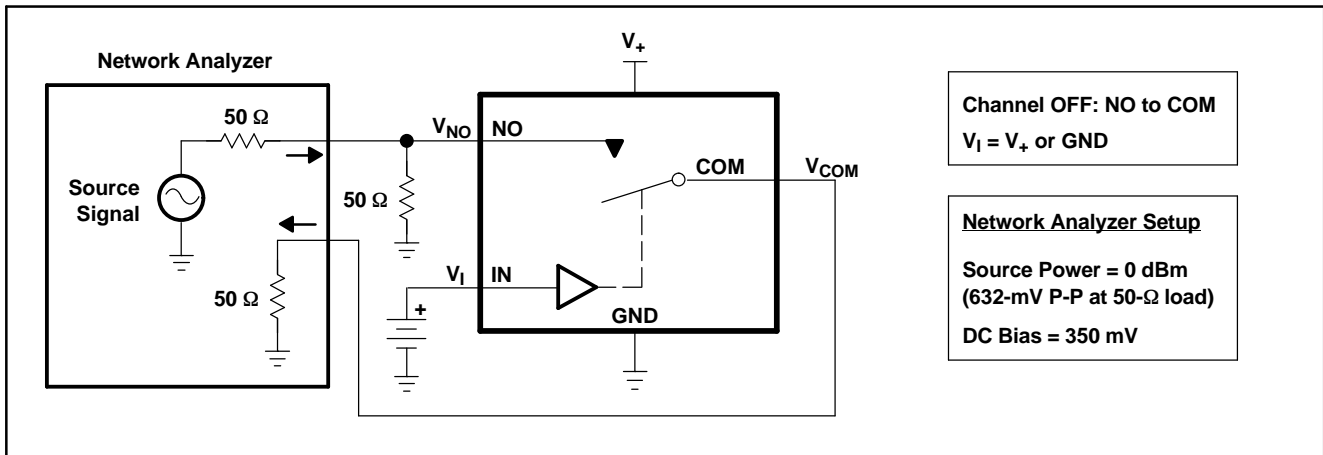


Figure 19. OFF Isolation ( $O_{ISO}$ )

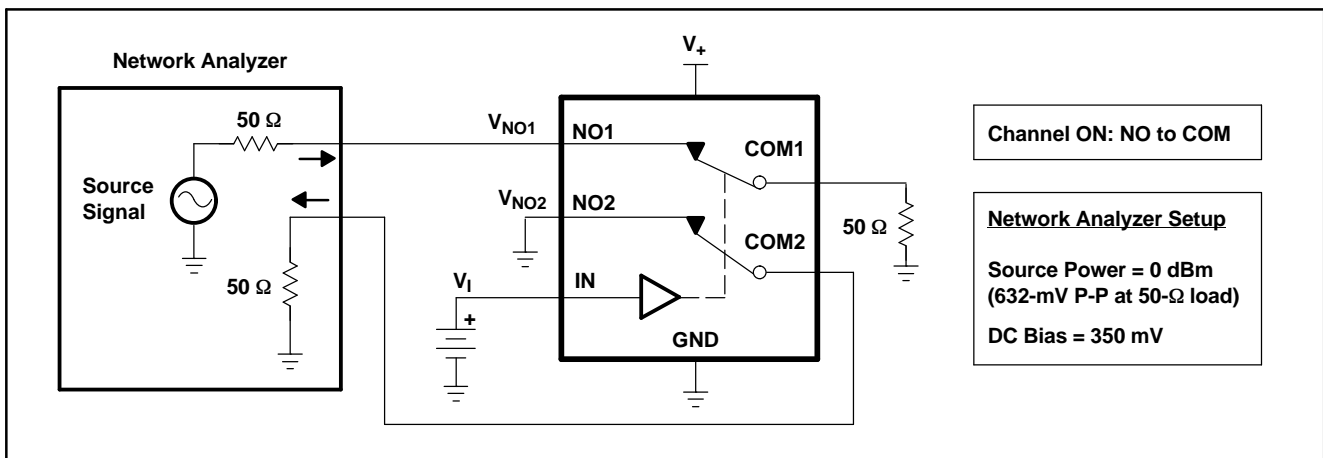
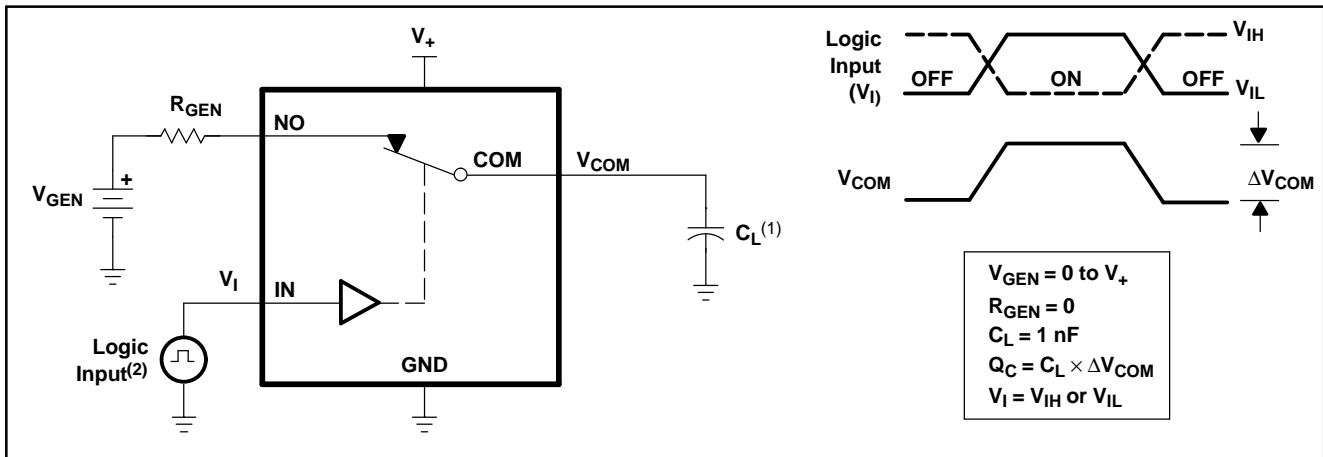


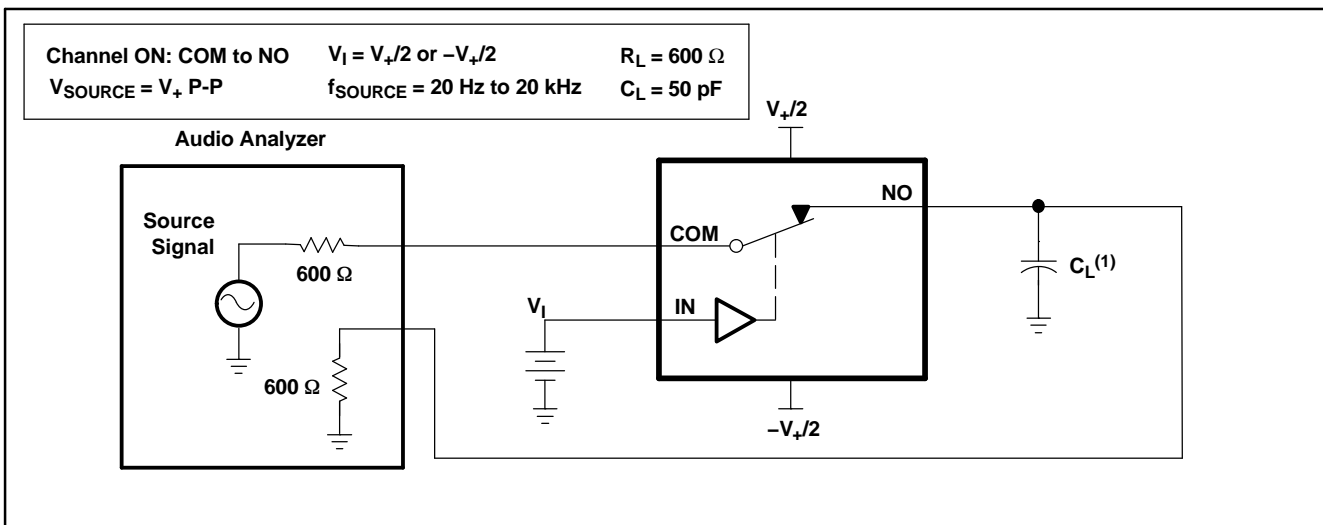
Figure 20. Crosstalk ( $X_{TALK}$ )



(1)  $C_L$  includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

**Figure 21. Charge Injection ( $Q_C$ )**



(1)  $C_L$  includes probe and jig capacitance.

**Figure 22. Total Harmonic Distortion (THD)**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS5A23166DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A23166DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A23166YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

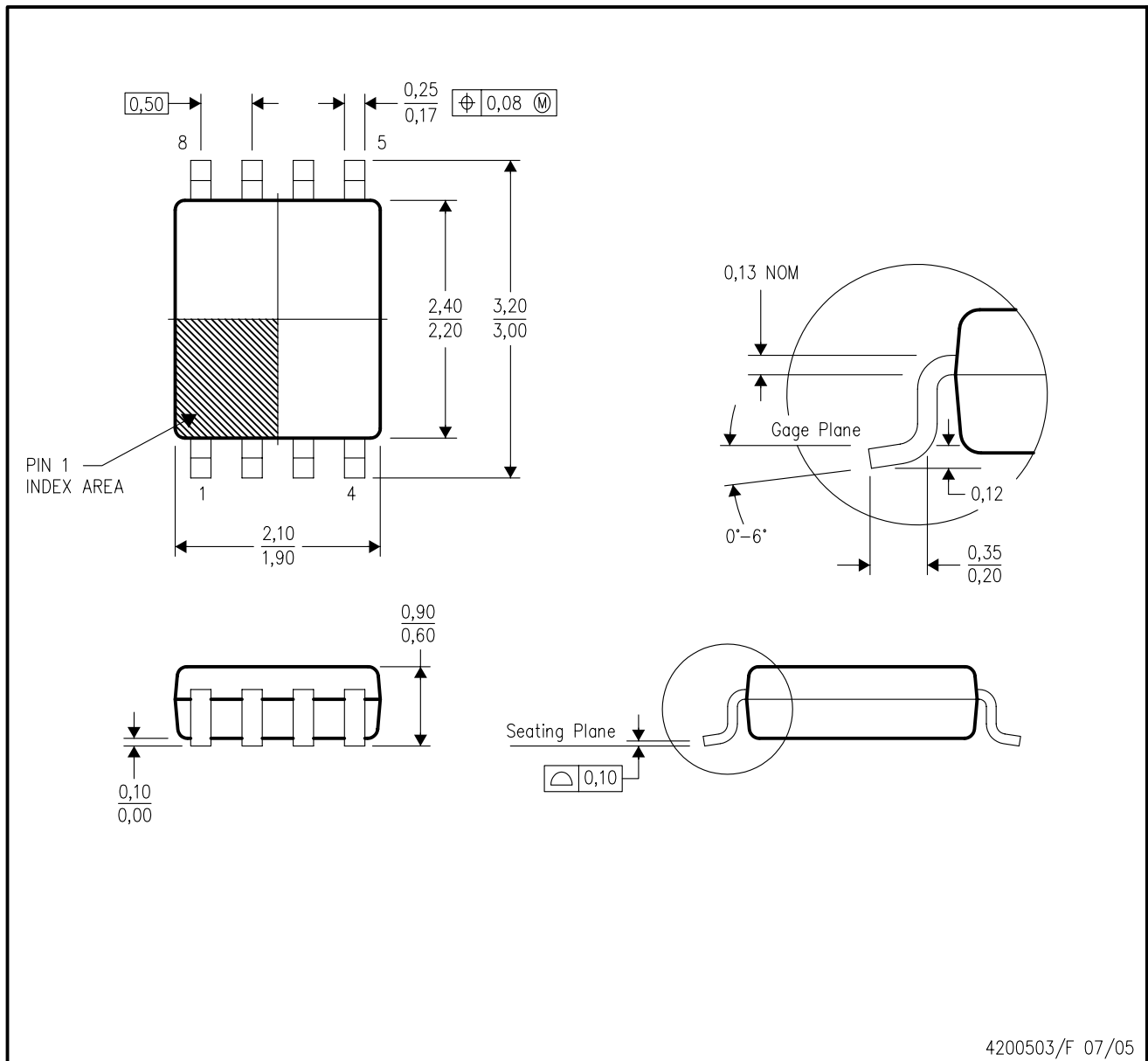
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCU (R-PDSO-G8)

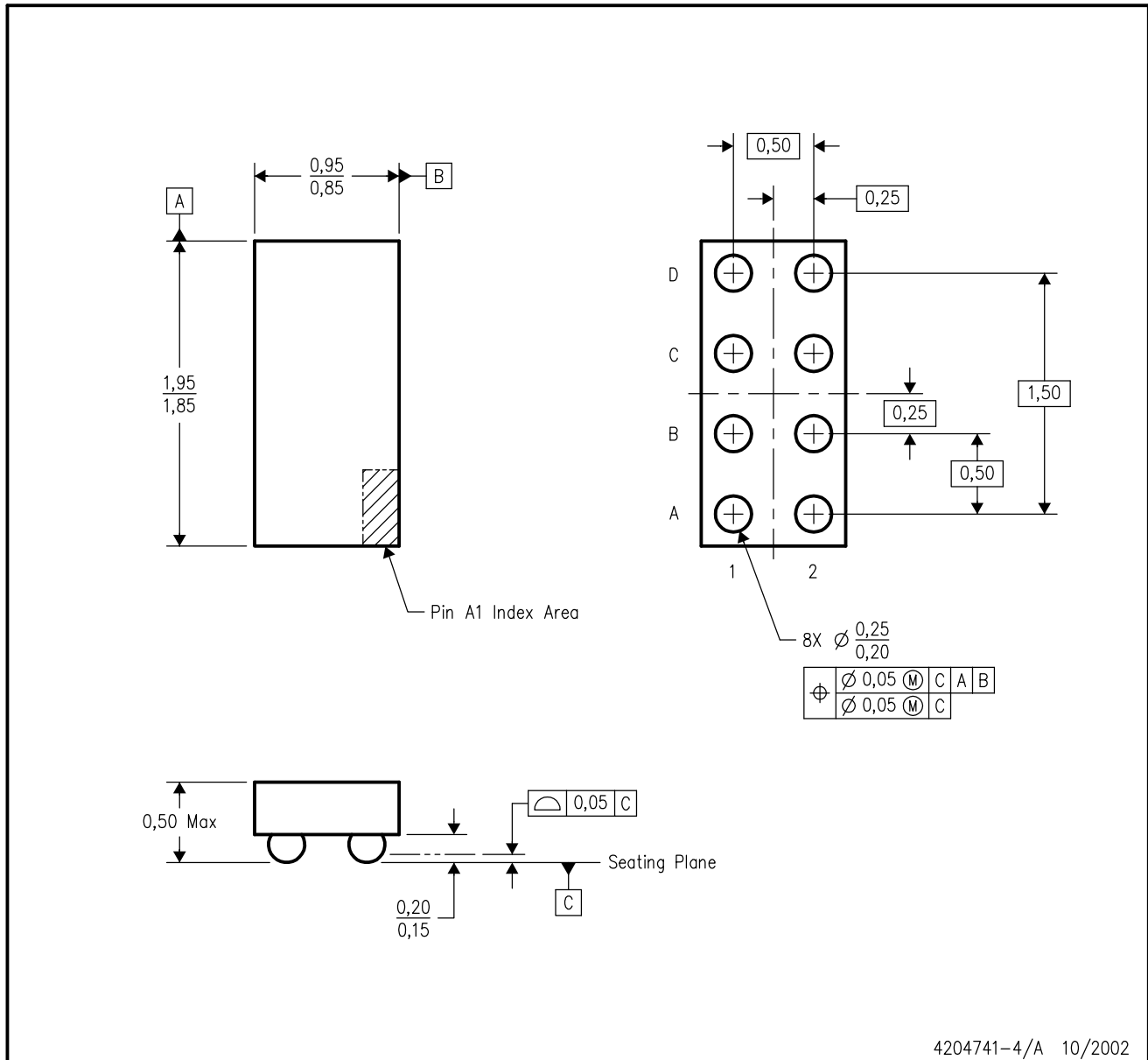
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-187 variation CA.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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